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L4: Entry 20 of 49 File: USPT Apr 13, 1993

DOCUMENT-IDENTIFIER: US 5202624 A
TITLE: Interface between IC operational circuitry for coupling test signal from internal test matrix

ABPL:
A programmable interface apparatus between a first circuit and either a second operational circuit, or a primary pin, of an IC includes a latch for receiving a test signal. The latch is controlled using probe lines and sense lines from an internal test matrix. In one configuration, such an interface is programmably configured to couple either a primary input signal or a test signal to the operational circuitry. In another configuration, such an interface is programmably configured to couple either an operational circuit signal or a test signal to a primary output pin. In still another configuration, such an interface is programmably configured to couple either an operational circuit signal or a test signal to an operational circuit element. In one embodiment, the interface is formed with a pair of transmission gates, the latch and an invertor. An advantage of such structure is the minimal IC area required. A global control signal is coupled to each transmission gate for configuring the interface for normal operation or test signal operation. For normal operation, an input signal is coupled directly to the interface output. For test signal operation, a test signal is applied to the interface output.

BSPR:
According to another test approach a grid-based test structure is integrated into the IC with the operational circuitry. Such a structure is described in commonly-assigned U.S. Pat. No. 4,749,947 issued Jun. 7, 1988 for GRID-BASED, "CROSS-CHECK" TEST STRUCTURE FOR TESTING INTEGRATED CIRCUITS. Such test structure enables access to internal operational circuit elements which are not directly accessible through the IC's primary pins. To further ease the test process, a programmable interface structure is needed which enables the test structure to access circuits at the operational circuitry boundary (e.g., circuit elements directly coupled to the primary pins). Further, a programmable interface for routing test responses off-chip through primary output pins is needed.

BSPR:
According to the invention, a programmable interface apparatus between operational circuitry of an IC includes a latch which couples a test signal from an internal test matrix to the operational circuitry. The interface is controlled using a single internal, global control line to couple either an operational signal or a test signal to the operational circuitry. The interface may couple one operational circuit element to another or may couple a primary pin to an operational circuit element.

BSPR:
According to one aspect of the invention, a latch controlled by signals from the internal test matrix is used to couple a test signal from internal test structure to operational circuitry or a primary pin through the interface. The test matrix signals include probe lines and sense lines. A probe line enables the latch, while a sense line writes a logic state (e.g., test signal) into the latch. Such probe lines and sense lines also are used for setting logic states at internal circuit elements. An advantage of using the probe lines and sense lines to control the latch is that race conditions between the test signal and an operational signal are avoided during testing. An advantage of using a simple latch is that minimal chip area is required. Another advantage of the latch is that test signals are loaded serially without the need for complex scan registers.

BSPR:
According to another aspect of the invention, the interface couples a primary input pin to operational circuitry. Such interface is programmable enabling a test signal to be applied to the operational circuitry in place of a signal received at the primary input pin. Such test signal is received from an internal test matrix.

BSPR:
According to another aspect of the invention, the interface couples operational circuitry to a primary output pin. Such interface is programmable enabling a test signal to be applied to the primary output pin in place of the signal from the operational circuitry. Such test signal is received from internal test circuitry and for example, may be a test signal response routed from some internal circuit element through the internal test structure and interface.

DEPR:
FIG. 2 shows a conventional test matrix 18 as described in commonly-assigned U.S. Pat. No. 4,749,947 issued Jun. 7, 1988 for GRID-BASED, "CROSS-CHECK" TEST STRUCTURE FOR TESTING INTEGRATED CIRCUITS. The test matrix 18 is formed of individually accessible probe lines 32 and control/sense lines 34 with electronic switches 36 at the crossings. A probe line 32 is coupled to a switch 36 for defining the switch "ON" or "OFF" state. One conducting channel of the switch 36 is coupled to a test point 38, while another conducting channel is coupled to a control/sense line 34. Each test point is coupled to one or more internal operational circuit elements 17 of the operational circuitry 16. FIG. 2 shows operational circuitry gates G coupled to respective test points 38.

DEPR:
Each control/sense line 34 is coupled to the data register 22 (FIG. 1) via a sense receiver / control driver (not shown). When the sense driver is inactive, the line 34 functions as a sense line for monitoring a response signal from the test point 38. When the control driver is active, the line 34 functions as a control line along which a control signal is conducted toward a test point 38. Activating a select switch 36 through a corresponding probe line 32 enables a test point 38 to be sensed or controlled.

DEPR:
The IC 10 is tested by applying respective control signals to select test points 38 and sensing respective response signals from other select test points 38. To apply a control signal to a select test point 38, the instruction register 20 is loaded. The instruction register 20 in response activates a select probe line and enables an appropriate control driver/sense receiver to function as a driver. The control signal then is read from a corresponding bit of the data register 22, and fed through switch 36 to the select test point 38.

DEPR:
To sense a response signal from a select test point 38, the instruction register 20 activates a select probe line and sets an appropriate control driver/sense receiver to receiver. The response signal then is read from the select test point 38 through switch 36 into data register 22.

DEPR:
The steps of driving a control signal and monitoring a response signal at different test points are accomplished with one or more instructions loaded into instruction register 20. A first instruction may activate a first probe line and first control line, while a second instruction activates a second probe line and second sense line.

DEPR:
As shown in FIG. 3, interface 12 receives signals C, S1, S2, P1 and P2 from the test matrix 18. Signal C is a global control line connected to each interface 12 for switching the interface between normal operation in which a signal IN is passed from driver 40 to driver 42 and alternate signal operations in which a substitute signal is applied to driver 42. Signals S1 and S2 are sense/control line signals from the test matrix 18. Signals P1, P2 are probe line signals from the test matrix 18. Test matrix transistors 58, 60 also are shown. When probe line signal P1 is active (e.g., active low), sense line signal S1 is passed through transistor 58. When probe line signal P2 is active (e.g., active low),

sense line signal S2 is passed through transistor 60.

DEPR:
Invertors 46, 48 and transistor 57 are configured as a latch circuit 68. The output of the latch 68 is coupled to the transmission gate 64. A data input to the latch is received from the drain of transistor 60. When probe line signal P2 is active (e.g., active low), the value of the sense line signal S2 is input to latch 68 at invertor 46. When probe line signal P1 is active (e.g., active low), the sense line signal S2 is output to the transmission gate 64. When probe line signal P1 is inactive (e.g., high), the latch contents do not change.

DEPR:
A test signal is routed to the interface output, driver 42 when the control signal C is at a second logic state (e.g., C=1). For an interface 12 coupled to a primary input pin 14, a test signal (to the signal IN) is passed from the interface 12 to the driver 42 and into the operational circuitry 16. To apply such test signal, the test signal value is loaded into latch 68 from sense line S2 by applying active probe line P1 and P2 signals (e.g., logic zero). With the desired test signal value loaded at the latch, the value then is transmitted through gate 64 to driver 42 and operational circuitry 16 by setting the global control signal C to the second logic value (e.g., C=1).

DEPR:
For an interface 12 coupled to a primary output pin 14, a test signal (to the signal IN) is passed from the interface 12 to the driver 42 and primary output pin 14 when control signal C is at the second logic state. To apply such test signal, the test signal (sense line signal S2) value is loaded into latch 68 by applying active probe line P1 and P2 signals (e.g., logic zero). With the desired test signal value loaded at the latch 68, the value then is transmitted through gate 64 to driver 42 and primary output pin 14 by setting the global control signal C to a logic one.

DEPR:
To allow the test matrix 18 to test the interface 12, additional functions as listed above in Table A also are performed. By setting the probe line signal P1 active (P1=0) and the probe line signal P2 inactive (P2=1), the value at node 65 is sensed. Such value is received into transistor 58 and read by the data register as sense line signal S1. By performing such function while C=0 (normal operation), the value sensed is the value of signal IN if the interface is performing properly. By performing such function while C=1, the value sensed at node 65 is the value stored in the latch if the interface is performing properly. Thus, a value can be loaded in the latch (P1=0, P2=0), then read out (P1=0, P2=1) as sense line signal S1 to test one path through the interface; or loaded with a value through the primary input pin 14, then read out (P1=0, P2=1) as sense line signal S1 to test the other path through the interface.

CLPR:
1. An interface apparatus integral to an IC coupling an IC primary pin to IC operational circuitry, the IC having an internal test structure including a grid of probe lines and sense lines, a probe line and a sense line being coupled to the interface apparatus, the interface apparatus comprising:

CLPR:
3. An integrated circuit having primary I/O pins, operational circuitry, a built in test structure, and interface apparatus, the test structure including a grid of probe lines and sense lines, a probe line and a sense line being coupled an interface apparatus, each interface apparatus coupling a primary I/O pin to the operational circuitry, an interface apparatus comprising:

CLPR:
5. An interface apparatus integral to an IC for coupling a first operational circuit element of the IC to a second operational circuit element of the IC, the IC having an internal test structure including a grid of probe lines and sense lines, a probe line and a sense line being coupled to the interface apparatus, the interface apparatus comprising:

CLPV:
a latch receiving a test signal from a sense line for latching said test signal, the latch coupled to a probe line which controls latching of the latch;

CLPV:
a latch receiving a test signal from a sense line for latching said test signal, the latch coupled to a probe line which controls latching of the latch;

CLPV:
a latch for latching a test signal received from one of said sense lines, the latch coupled to one of said probe liens wherein said probe line controls latching of the latch;

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L13: Entry 1 of 51 File: USPT Aug 22, 2000

DOCUMENT-IDENTIFIER: US 6107821 A
TITLE: On-chip logic analysis and method for using the same

ABPL:
A programmable logic device (PLD) includes a plurality of logic resources, a plurality of multi-bit configuration memories (MBCMs), and a trigger logic structure. The plurality of MBCMs include multiple memory slices that allow the PLD to switch rapidly between configurations, or contexts. In one embodiment, at least one memory slice configures the PLD into a logic analysis context for providing on-chip testing. In one embodiment, the plurality of logic resources include a plurality of storage elements. State data generated by a user-defined context is stored in the plurality of storage elements. When the trigger logic structure provides a trigger signal, the PLD is reconfigured into the logic analysis context. The logic analysis context reads and processes the state data stored in the plurality of storage elements to test the performance of the user-defined context. In one embodiment, the storage elements are multi-bit micro-registers that store state data generated by a plurality of contexts implemented in the multiple-context PLD.

BSPR:
In accordance with an embodiment of the present invention, a multiple-context PLD comprises a plurality of logic resources, a configurable interconnect structure (CIS) for interconnecting the logic resources, a plurality of multi-bit configuration memories (MBCMs), and a trigger logic structure. The plurality of MBCMs are programmed such that at least one context of the multiple-context PLD provides a desired user context (DUC) to be tested, while at least one other context provides an on-chip logic analysis context (LAC). During operation of the DUC, a trigger signal from the trigger logic structure causes the multiple-context PLD to be reconfigured into the LAC. In one embodiment of the invention, the logic resources include storage elements (e.g., micro-registers) for storing state data associated with one or more DUCs. By reading the state data from the DUC stored in the micro-registers of the logic resources, the LAC can analyze the performance of the DUC. Upon completion of the testing process, the multiple-context PLD is reconfigured back into the DUC and normal operation resumes. The results of the testing process can be immediately provided to the pins of the multiple-context PLD, or can be stored in a test data storage element of the multiple-context PLD for a subsequent batch output process.

DEPR:
FIG. 4 shows an FPGA 400 that represents one of several Programmable Logic Device (PLD) types. FPGA 400 comprises a user-configurable logic structure (UCLS) 450, a configuration control circuit 430, a configuration port 420, a trigger logic structure 460, a test data storage element (TDSE) 440, and a plurality of multi-bit configuration memories (not shown). UCLS 450 includes a plurality of configurable logic blocks (CLBs) 402, a plurality of input/output blocks (IOBs) 404, and a configurable interconnect structure (CIS) 410. CIS 410 comprises a plurality of programmable switch matrices (PSMs) 406 that control the routing of signals between CLBs 402 and IOBs 404.

WEST

Generate Collection

L14: Entry 1 of 4 File: USPT Aug 22, 2000

DOCUMENT-IDENTIFIER: US 6107821 A
TITLE: On-chip logic analysis and method for using the same

ABPL:
A programmable logic device (PLD) includes a plurality of logic resources, a plurality of multi-bit configuration memories (MBCMs), and a trigger logic structure. The plurality of MBCMs include multiple memory slices that allow the PLD to switch rapidly between configurations, or contexts. In one embodiment, at least one memory slice configures the PLD into a logic analysis context for providing on-chip testing. In one embodiment, the plurality of logic resources include a plurality of storage elements. State data generated by a user-defined context is stored in the plurality of storage elements. When the trigger logic structure provides a trigger signal, the PLD is reconfigured into the logic analysis context. The logic analysis context reads and processes the state data stored in the plurality of storage elements to test the performance of the user-defined context. In one embodiment, the storage elements are multi-bit micro-registers that store state data generated by a plurality of contexts implemented in the multiple-context PLD.

BSPR:
The logic resources of a conventional PLD can be configured to provide a logic analysis circuit, i.e., a circuit that provides stimulus for, observes, and/or analyzes logic values in a circuit under test. However, a conventional PLD is generally heavily utilized, leaving few, if any, available logic resources free for the logic analysis circuit. This resource limitation dictates that the logic analysis circuit be external to the PLD (off-chip). However, the state data from the test nodes in the PLD must still be distributed to the external logic analysis circuit at appropriate times. In a conventional PLD, a portion of the logic resources are configured as "probe circuits", which provide both triggering functions and the transference of state data from the test nodes to various pins. Although the probe circuits consume a portion of the available logic and routing resources, this portion is much smaller than would be required by a logic analysis circuit.

BSPR:
FIG. 2 shows a conventional FPGA 200 having a portion of its logic and routing resources configured as probe functions. FPGA 200 is similar to FPGA 100, comprising CLBs 102a-102i surrounded by IOBs 104a-104l, a CIS 110, a configuration port 120, and a configuration control circuit 130. CLBs 102b and 102f and IOBs 104b and 104e (shown shaded) are configured to provide probe circuits for testing of the UC in the remaining CLBs and IOBs.

BSPR:
The use of probe circuits to gather the data for verification of a UC provides great flexibility in the selection of trigger logic and test nodes. The logic and routing resources used to provide the probe circuits are from the same pool of resources used by the active UC. Therefore, the probe circuits have direct access to the test nodes of the active UC.

BSPR:
However, the use of otherwise general-purpose CLBs and IOBs to create the probe circuits reduces the logic and routing resource available for the desired UC. Therefore, in heavily utilized PLDs, resource limitations may curtail the effectiveness of probe circuit testing. Either a reduced number of probe circuits may be used to perform partial testing of the UC,

BSPR:
or the UC itself may be only partially configured (i.e., portions of the desired logic may be eliminated from the UC), to make additional logic and routing resources available for the probe functions. Neither option is completely satisfactory. Partial testing can be time-consuming if multiple test runs must be made to cover the full range of UC operation. In addition, partial testing may fail to detect problems associated with the full UC. On the other hand, partially configuring the UC can potentially alter the performance of the UC. Further, the inclusion of probe functions in the PLD along with the UC can affect the performance of the UC. The additional gates, gate activity, and routing modifications can generate noise and signal delays in the UC, leading to erroneous test results.

BSPR:
Another problem associated with probe function testing is that a large number of pins may be required to transmit the state data to the external logic analyzer. Typically, one pin is used to transfer the state data from each test node being examined. The active UC requires a certain number of pins for its own data input/output activity. Because the total number of pins in a PLD package is limited, typically either the UC must be modified or the test abridged.

BSPR:
An alternative method for testing the operation of a UC is the Readback process, developed by Xilinx, Inc. and used in their XC4000.TM. series FPGAs. The Readback process addresses some of the resource limitation and signal delay issues of probe circuit testing. FIG. 3 shows a simplified circuit diagram of an FPGA 300, which is consistent with the XC4000-series FPGAs from Xilinx, Inc. FPGA 300 is similar to FPGA 100 (FIG. 1), and comprises an array of CLBs 102 surrounded by a ring of IOBs 104 and interconnected by a CIS 110 including multiple PSMs 106. As in FPGA 100, CLBs 102, IOBs 104, and PSMs 106 in FPGA 300 are configured by a configuration control circuit 130 using data received through a configuration port 120. However, FPGA 300 further includes readback logic resources 302 and readback routing resources 304. Readback logic resources 302 comprise a trigger net (not shown) that can be connected to any IOB 104 by readback routing resources 304. When a low-to-high transition takes place on the trigger net, readback logic resources 302 begin shifting out a data stream that reports the configuration bits of FPGA 300. Readback logic resources 302 can be configured to also include the contents of all flip-flops and latches in FPGA 300 in the readback data stream. This data stream is fed to an IOB that routes the data stream to an external logic analyzer (not shown).

BSPR:
In accordance with an embodiment of the present invention, a multiple-context PLD comprises a plurality of logic resources, a configurable interconnect structure (CIS) for interconnecting the logic resources, a plurality of multi-bit configuration memories (MBCMs), and a trigger logic structure. The plurality of MBCMs are programmed such that at least one context of the multiple-context PLD provides a desired user context (DUC) to be tested, while at least one other context provides an on-chip logic analysis context (LAC). During operation of the DUC, a trigger signal from the trigger logic structure causes the multiple-context PLD to be reconfigured into the LAC. In one embodiment of the invention, the logic resources include storage elements (e.g., micro-registers) for storing state data associated with one or more DUCs. By reading the state data from the DUC stored in the micro-registers of the logic resources, the LAC can analyze the performance of the DUC. Upon completion of the testing process, the multiple-context PLD is reconfigured back into the DUC and normal operation resumes. The results of the testing process can be immediately provided to the pins of the multiple-context PLD, or can be stored in a test data storage element of the multiple-context PLD for a subsequent batch output process.

DRPR:
FIG. 2 is a simplified circuit diagram of a conventional FPGA configured to include probe function capability.

DEPR:
FIG. 4 shows an FPGA 400 that represents one of several Programmable Logic Device (PLD) types. FPGA 400 comprises a user-configurable logic structure (UCLS) 450, a configuration control circuit 430, a configuration port 420, a trigger logic structure 460, a test data storage element (TDSE) 440, and a plurality of

multi-bit configuration memories (not shown). UCLS 450 includes a plurality of configurable logic blocks (CLBs) 402, a plurality of input/output blocks (IOBs) 404, and a configurable interconnect structure (CIS) 410. CIS 410 comprises a plurality of programmable switch matrices (PSMs) 406 that control the routing of signals between CLBs 402 and IOBs 404.

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L17: Entry 8 of 15 File: USPT Sep 28, 1999

DOCUMENT-IDENTIFIER: US 5960191 A
TITLE: Emulation system with time-multiplexed interconnect

DEPR:
Signals contributing to events are latched by the same scan flip-flops 2004 used for logic analyzer data and previously shown in FIG. 20b. These signals are then routed to JTAG programmable edge detectors comprising CLB memories 2018 (CLB memory is memory available on the logic chips 10, 204) which are then AND'ed together using wide edge decoder 2012 to form eight event signals. The eight event signals inside each logic chip 10, 204 are combined two to a pin using multiplexer 2020 and output to the emulation board as event signals 236 (also shown in FIG. 20a) where they are again AND'ed with the event signals from other FPGAs. The board level event signals are transmitted over the backplane to the control board where they are AND'ed with event signals from other emulation boards and other boxes. The resulting system wide event signals go the trigger logic chip 674 on the control board where they are used to generate an acquisition enable and other logic analyzer control signals.

L20: Entry 19 of 50 File: USPT Jan 10, 1995

DOCUMENT-IDENTIFIER: US 5381420 A
TITLE: Decoupled scan path interface

ABPL:
An interface to internal scan paths within an IC for synchronizing a test clock and a system clock without adversely affecting their operation. The test clock provides input test data (TDI) to the interface and receives output test data (TDO) from the interface at the test clock rate. The system clock drives the test data through the scan path at the system clock rate. The two clocks are "decoupled" in that they run independently, being synchronized by the interface for clocking the test data into, through and out of the scan path. In effect, the interface decouples the internal scan paths driven by the system clock from the test logic driven by the test clock. This feature enables the IC to be tested "at speed" and provides for synchronization between the test clock and system clock over a wide range of test clock frequencies.

BSPR:
Historically, traditional methods of testing printed circuit boards (PCBs) have required physical contact of an array of test probes with pins of integrated circuit packages (ICs) mounted on the boards. This array of test probes, called a "bed-of-nails," tests interconnections on a board between ICs by forcing an output pin on an IC to a test value and then sampling an input pin of a connected IC to see if it received the test value. Bed-of-nails can also test internal paths within an IC by forcing input pins to test values and sampling the results at output pins for comparison against ideal results.

BSPR:
However, the bed-of-nails approach does not work for surface mounted devices (SMDs) or VLSI circuits that have minimal spacing between pins. SMDs are mounted directly to the surface of the PCB and do not have pins that extend through the board for a probe to contact. Moreover, SMDs are often mounted on both sides of the board, further complicating testing of the IC. VLSI circuits can have as little as 15 thousandths of an inch between pins, making it virtually impossible to attach a probe to a pin.

BSPR:
In response to the need for an all-electronic approach to testing, the industry has developed a standard test architecture known informally as the JTAG standard and formally as the IEEE 1149.1 standard. This standard test architecture supports board-level testing using a bus that connects to boundary-scan test logic in each IC. The term "boundary scan" means that the input and output pins (I/O pins), or boundaries, of the IC may be stimulated/monitored electronically during a test. The test logic includes boundary scan registers for allowing test data to be electronically placed on an output pin or to be observed on an input pin without the need for physical contact by a probe. It also includes a test access port (TAP), within the IC which serves as an interface between test data registers (such as a boundary scan register) on the IC and the bus. However, the JTAG standard goes further. It includes permission for users to add and access other scan registers, or scan paths, within an IC to test the internal operation of the IC. This is a powerful option, since it addresses a common need to provide for the complete testing of integrated circuit embedded within an assembled electronic system.

BSPR:
The common approach for testing ICs that comply with the JTAG standard and provide access to internal scan paths is to temporarily substitute the JTAG test

clock for the IC's normal system clock during testing of the internal scan path. The test clock "drives" the internal scan path during test and the system clock drives the scan path during normal operation. This switching between the two clocks is known as multiplexing and is easily done. However, there are several disadvantages to clock switching. First, the switching of clock signals raises risks of unreliable or false clocking and excessive clock slew, particularly for application-specific-integrated circuits (ASICs). Second, clock switching does not allow for "at-speed" testing. Instead, tests are executed at the test clock frequency, which is usually only a fraction of the system clock frequency in modern high-performance electronic systems. Unlike the system clock frequency, the test clock frequency is often constrained by such system-level concerns as high fan out clock distribution/skew and noise/susceptibility related to fast logic edge rates. And third, there is a growing demand, fueled by the advent of multi-chip module (MCM) technology, to test ICs at their maximum speeds before they are mounted in a module. Testing device limitations often make this testing of such ICs with the clock switching technique impractical.

BSPR:
The invention provides an interface to internal scan paths within an IC which synchronizes the test clock and the system clock without adversely affecting their operation. The test clock provides input test data (TDI) to the interface and receives output test data (TDO) from the interface at the test clock rate. The system clock drives the test data through the scan path at the system clock rate. The two clocks are "decoupled" in that they run independently, being synchronized by the interface for clocking the test data into, through and out of the scan path. In effect, the interface decouples the internal scan paths driven by the system clock from the test logic driven by the test clock. This feature enables the IC to be tested "at-speed" and avoids the other disadvantages of the clock switching approach. Furthermore, in a preferred embodiment, the interface is versatile in providing synchronization between the test clock and system clock over a wide range of test clock frequencies.

DEPR:
The output of the synchronizer/edge detector 24a and scan control register 26 are routed to the scan control decoder 28 that also receives the output of the scan control counter 20. The decoder 28 generates the signals SCAN and HOLD, which provide control for internal scan paths. Depending on the type of current instruction, these signals may be controlled by a scan instruction, a halt/single step instruction or a trigger register 30 (breakpoint instruction). The trigger register 30, clocked by the system clock, allows the state of the IC under test to be frozen based upon a trigger event defined in the system. Trigger events may be defined by external strobes, state comparators, occurrence counters, or some combination of these conditions.

DEPR:
Most ICs under test will have designed into them a number of scan paths for testing different portions of the circuit design. The scan control register 26 thus receives a Scan Path Select signal from the testing device, synchronizes it to the system clock and routes it to a scan path select multiplexer 32. The multiplexer 32 selects the last 2N bits from one of the scan paths as determined by the register 26.

DEPR:
On the output side of the interface the last N bits from the internal scan path are copied in parallel to the output scan cache 36 at the same time that the N bits in the input buffer 12 are copied to the input scan cache 14. Therefore, during the subsequent N test clock cycles, the modulo-N Counter 16 also selects the appropriate bit from cache 36 via the output scan multiplexer 40 to serve as the test data output (TDO) for the IC.

DEPR:
In one approach, the scan path may be evaluated whenever the TAP controller enters the Run/Test-Idle state and an internal scan instruction is current. This approach, which is depicted in FIG. 1, does not generally provide for at-speed testing of the internal IC logic.

DEPR:
The benefit provided by the hold proviso is that it allows a global halt/single-step capability to be added to the IC design. Using dedicated JTAG

instructions and/or specialized trigger logic, the hold and scan enable signals can be interactively controlled to halt the state of the IC on a given condition (internal or external), to inspect the IC's internal contents without disturbing them, to selectively modify the IC's contents, or to single-step the IC through a given set of operations. This final capability is particularly attractive in the design of processing elements. Therefore, the invention inspires an overall on-line test and diagnostic environment for integrated circuits.